Improve Productivity

SPECIFICATIONS

Parallel Test:	64 DUT sites, 32 DUT sites and 16 DUT sites
Test Frequency:	Up to 400Mhz
I/O Interface:	ONFI 1.0, 2.0 or above
Clock Lines:	3 pairs per DUT site
Address Depth:	65536 Blocks, 8192 Pages and 8192 Columns per site, up to 8 sites
Data Width:	x8, x16 and x32 per DUT site
Control Lines:	4 CS, 1 RE, 1 ALE, 1 WP, 1 RYBY, 1 CLE, 1 WE
Programmable Timing:	tCLS, tCLH, tALS, tALH, tWP, tWH, tDS, tDH, tDS, tDH, tWC, tADL, tCH, tWW, tCS, tRP, tRC, tREA, tRR, tOH, tWHR, tAR, tWB, tREH, tBERS, tR, tPROG
Variable Power Supplies:	Vdd: 1.20V to 3.8V, resolution 0.01V, 4A, +/- 2%, per DUT site
Leakage Current Measurement: (Based on each site measurement per pin)	R1: 0uA - 10uA, +/- 1uA R2: 10uA - 100uA, +/- 2uA R3: 100uA - 1mA, +/- 25uA R4: 1mA - 40mA, +/- 450uA
Operating Icc Measurement: (Based on each site measurement)	R1: 0 - 3A (+/- 50mA) R2: 3 - 10A (+/- 100 mA)
Stand-by Icc Measurement: (Based on each site measurement)	R1: 0uA - 10uA, +/- 1uA R2: 10uA - 100uA, +/- 2uA R3: 100uA - 1mA, +/- 25uA R4: 1mA - 40mA, +/- 450uA
Min. Control PC:	Windows XP+ and networking interface

TRIAD SPECTRUM

Your Memory Tester Partner

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TRIAD SPECTRUM

Your Memory Tester Partner

Extend the range of your NAND FLASH testing with TurboCATS III-1200N

What we do?

The TCIII-1200N can be used as a production tool as well as an engineering tool. With the standard industry test patterns available such as Checkerboard and Marching, for use in your testing process, there is no problem selecting the right patterns for your particular needs. In addition to the DC testing, the TCIII-1200N also supports AC testing. The AC testing feature will allow the end user to program test patterns using the script coding method.

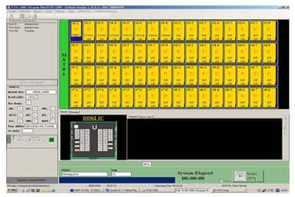
In a production environment throughput is the key.

The TCIII-1200N comes with 64 sites to assist you in this process. 64 IC can be tested in parallel in order to provide a faster production. Error logging on Block/Page/Column and DQ's is also available.

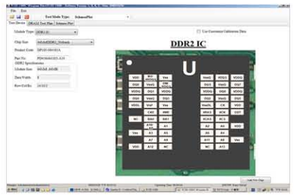
TCIII-1200N NAND Flash

EMPOWER

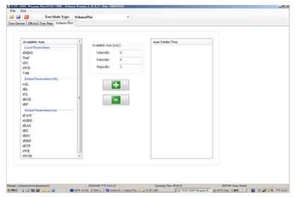
your business with advanced technology.



Main Screen



Test Device



Schmoo Plot

ENHANCED BUS SPEED

TCIII-1200N NAND Flash

- NAF - ONFI 1.0, 2.0 or above
- Maximum operating clock frequency 400Mhz
- Supports both large block and small block architecture
- Supports AC/DC parametric tests
- User Script Code programming for customized test patterns (optional)
- Built in Icc patterns include sequential read operating current, program operating current, erase operating current and stand-by current (TTL)
- Leakage pin and Continuity test
- AC tests include read ID, erase, program, read, mark bad blocks and read bad blocks
- Supports Block/Page/Column modes
- Supports cache read, sequential read and copy back
- Flexible bad block management available for read bad block
- Over 35 industry standard AC test patterns available
- Over 20 AC timing parameters for AC parametric testing

PATTERN GENERATOR

SCRIPT CODE FUNCTION

- Older model Triad Spectrum test systems provided a wide variety of AC test patterns but did not allow the user to generate a proprietary test pattern. The new TCIII-1200N offers the "Script Code" feature. This will let the end user to program proprietary test patterns.

  Utilizing the script programming language, the customer can create a customized test pattern and then use the Script Code pattern generation compiler to compile and generate the new test pattern. The new pattern is then imported into the test list with AC (tADL, tALH, tALS, tCH, tCS, tAR, tRC, tR, tBERS, tPROG, etc) and DC (Vforce, Vcc) parameters for customized testing.

ENHANCED TIMING BUS

- Script Code programming gives the end user a great deal of flexibility in programming the timing bus to create a unique Read and Write bus transaction under best and worst case AC parameters. In addition, a "no wait" state bus transaction can be created in the Read to Write cycle.

POWER DEBUG/COMPILER TOOL

- A built in compiler and debuger environment is in the Script Code programming. This allows the user to monitor the timing waveform of the programming algorithm and the timing bus transactions under the Signal Tap tool.