

BusXpert Gen 3 PCI Express® Analyzer

FEATURES & BENEFITS

- Accurate capture of all data line rates including 8 GT/s, 5 GT/s and 2.5 GT/s
- Decode all PCI Express traffic including TLP, DLLP and ordered sets
- Interposers supported includes: slot (adapter cards), M.2 and U.2 interposers
- Portable and lightweight dedicated appliance; no need to hassle with and waste time swapping blades or modules
- Flexibility of using a gigabit Ethernet or USB 3.0 communication interface

ADVANTAGES

- .5 ps clocking resolution provide precise capture and recording sequences
- Easily search for specific frames, primitives, ordered set, addresses or other events with the Quick Search and Advanced Search functions
- Sophisticated triggering interface allows for quick definition of events with frame lavouts matching the PCI **Express specifications**
- Industry largest buffer; capture and analyze more with support for up to 72GB of trace buffer

The SerialTek BusXpert PCI Express (PCIe) analyzer is the industry's first analyzer designed and optimized for equipment manufacturers that are developing storage products and solutions using proven PCI Express technology. Supporting data rates of 2.5 GT/s, 5.0 GT/s (Gen 2) and 8.0 GT/s (Gen 3) and bus widths of x1, x2, x4



and x8, this advanced offering delivers unparalleled and accurate capture, analysis and insight of PCIe traffic at all layers of the protocol stack. It provides the same ease of use, multiple display views, powerful triggering and attractive price points that have long been hallmarks of SerialTek storage protocol products.

The BusXpert employs advanced technologies such as the industry's first Hardware Accelerated Gigabit Ethernet, pre-indexed and compressed trace data, multiple analysis processors, and instant display of the captured data. The analyzer provides for planned support for up to 144 GBs of capture buffer. Even the entry model that comes installed with 9 GBs of trace buffer has a deeper capture buffer than most competing analyzers. The BusXpert features easy to use triggering, pre/post-filtering, textual search and sequence search, and many different displays of captured PCI Express traffic.

Three probing options are supported. This includes a x1, x2, x4 and x8 slot interposer capability of supporting 5.0 GT/s and 8.0 GT/s data rates. The interposer permits PCIe traffic between a host system and a PCle card to be monitored, captured and analyzed. Additionally a M.2 interposer is available for M.2 socket 2 or M.2 socket 3 devices. The interposer when used with the BusXpert PCIe analyzer permits PCIe protocol traffic between a host system and a M.2/NGFF connector on a solid state device (SSD) to be monitored, captured and analyzed. This board support bus lane widths of x1, x2 as well as x4. The interposer also supports SSD lengths for 42mm, 60mm, 80mm and 110mm. Serialtek also offers a U.2 interposer. This interface is designed to be used to analyze PCIe traffic between a host backplane and dual ported SSDs. The interposer supports both 2.5" and 3" sized SSDs.

In addition to supporting the Gen2 and Gen3 PCIe standards, the analyzer supports the newer Non-Volatile Memory Express (NVMe) standard.

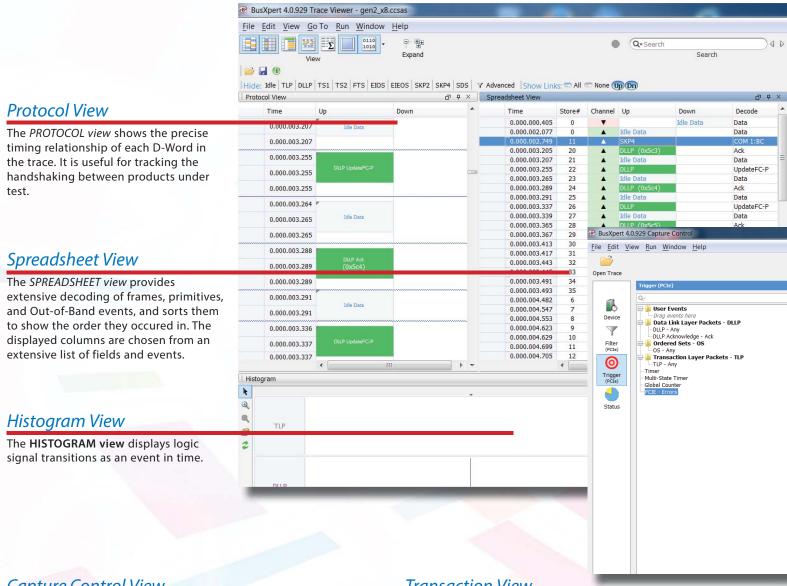
Simply put, no other PCIe analyzer packs so much power and so many features into a single solution. Find out today why leading storage manufacturers rely on SerialTek's product to accelerate development and test cycles.

As shown in the insert (page 2 and 3), the PCIe BusXpert software consists of a powerful set of GUI views that allow the user, to select and set-up an analyzer, prepare the analyzer for taking a trace, specifying and designing triggers and monitoring the trace. Once the trace is complete, a trace viewer is used to analyze the trace.

All analyzer functions and trace processing can be controlled from an API, which allows programmers to write custom analysis tools.



The BusXpert provides a variety of powerful traffic displays, with some optimized for different protocol layers, some optimized for time relationships, some correlate directly with the PCI Express specification, and some provide just the user data. All of the views are exportable via CSV and XML. Additionally, some can be exported to HTML. Bookmarks make it easy to label and discuss specific events in the trace.



Capture Control View

The CAPTURE CONTROL view allows the user to set up the analyzer for trace capture. The analyzer may be stopped in one of three ways: manual stop, buffer full, and by a trigger.

Filter View

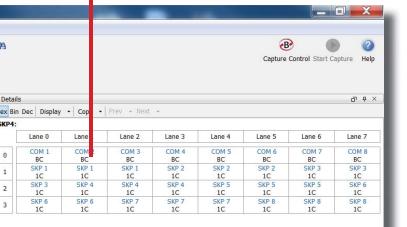
The FILTER view allows users to select items to be filtered from the trace. Filtered items are not part of the trace data and are not recoverable. Filtering is used to decrease unwanted items in the trace buffer allowing longer trace times to be taken. Items that are to be included in the trace are checked. Additional items can be added to the filter list through the "Options" menu.

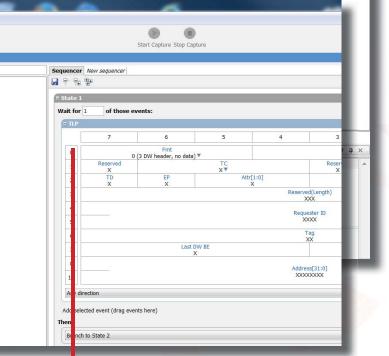
Transaction View

Frames may actually be scattered all over the trace (in time), but this view collects all the frames involved in a command and groups them together. Transactions can be expanded or collapsed, and the "Expand All"/"Collapse All" buttons on the main tool bar work in this view too (they only change the active view).

Frame Details View

The FRAME DETAILS view shows each frame in the format used by the PCI Express specification.



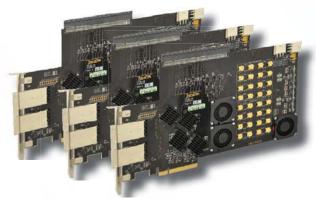


Trigger View

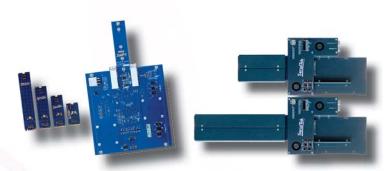
The TRIGGER view is where the user defines and builds the stop trigger. The trigger watches for a certain event (or sequence of events) and then causes the analyzer to stop after the fills according to the settings in the capture control view. Trigger sequences are defined by dragging trigger events into the sequencer menu. Events may be further edited and defined in the sequencer menu. PCIe events that are also supported include: TLPs, DLPs, Ordered Sets, Primitives, Timers and Global Counters. Within the sequencer, a user can define actions based on the event result. Actions include: Trigger, External Trigger Count, Count per Second, Increment Counter, Reset Counter and Branch to a New State.

New States may be defined within a trigger sequencer; many states can be defined within a trigger sequencer. Individual trigger sequencers may be defined in the trigger view. Trigger sequencers act independently and the first sequencer to trigger causes the analyzer to stop. Remaining sequencers do not cause triggers after the first sequencer triggers.

Tapping Methods and Interposers Supported

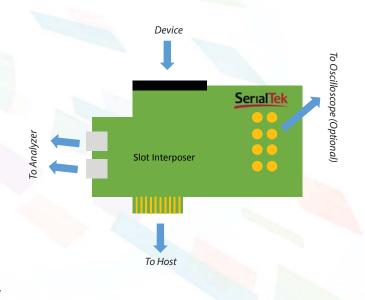


x1, x4 and x8 Slot Interposers with SMA Outputs



M.2 Interposer

U.2 Interposers



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The front panel LEDs are replicated in the Status view allowing LED status to be monitored remotely through the BusXpert software. Link utilization is graphed real time in terms of reads, writes and combined. Both bar graphs and speedometers display link utilization. Performance data may be logged into a specified user file. Data may be filtered by "clipping" or specifying the amount of data in each transfer to filter out. Buffer size can be specified as a % of the total buffer. When in trigger mode, users specify how much buffer space as a percentage is allocated to the trace before and after the trigger event. Buffer memory can be segmented into 1 to 256 segments. The trigger sequence is applied to each segment consecutively resulting in multiple captures without having to manually restart the analyzer.

A number of physical parameters in the analyzer are set in the capture control view. These include: Rate: Autodetect or Manual set Gen1, Gen2 or Gen3. Link Width: Autodetect or Manual Set x1, x4, and x8 Lane reversal Autodetect or Manual Set for both Upstream and Downstream device. Additionally. Polarity Inversion: Auto Invert Polarity or individual lane control for both Upstream and Downstream device.

SerialTek makes available the Analyzer in a variety of different configurations to meet varying corporate requirements for buffer size, protocols and budget. Contact us to schedule a demo and learn more. We also provide no obligation, no cost evaluation units.

Analyzer Specifications

Data Rates Supported	2.5 GT/s, 5.0 GT/s and 8 GT/s
PCIe Lanes Width	x1, x2, x4 and x8
Interposers Supported	Slot (3 versions), M.2 and U.2 (2 versions)
Trace Buffer (Maximum)	72 GBs (144 GBs planned)
Front Panel Connectors	4 SFF-8644 (SerialTek proprietary cabling), Trigger In, Trigger Out
Rear Panel Connectors	AC Power, Ethernet, USB3.0, 2 SATA Peripheral, Cascade
Downstream Status LEDs	Activity, TLP, ERR STS, CRC ERR Coding Err and Training, General
Status LEDs	Config, Ethernet, PCIe, USB, Run, Trigger
Front Panel Controls	Power ON/Off, Manual Trigger
Communication Interfaces	GigaBit Ethernet, USB 3.0
Dimensions	16" (depth) x 14" (width) x 3.5" (height) / 406mm x 356mm x 89mm
Weight	14.5 lbs / 6.6 kgs
Power	100-240VAC 47-63Hz; 500W Max Power
Environmental	Operating: 40 Degrees C Max Ambient Temperature

